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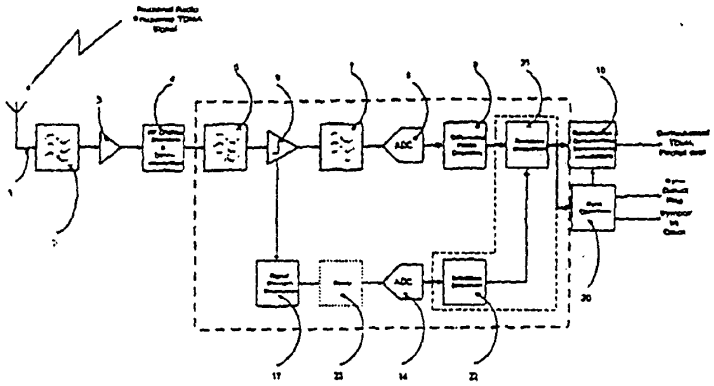

(57) Abstract

A receiver architecture is disclosed for use in Time–Division Multiple Access (TDMA) and related digital radio applications which combines the principal benefits of the conventional hard–limiting and linear receiver architectures to support switched–antenna diversity and multipath equalisation without the need for receiver gain control. A further feature of the receiver architecture is that minimises the dynamic range needed by the digital signal processing stages thereby reducing complexity, power consumption and cost compared to known arrangements. The (TDMA) radio frequency signal is separated into two components by the analogue section of the receiver: one component characterising the signal's phase, either absolute or differential, the second component characterising the signal's instantaneous magnitude. The (constant–envelope) phase componenet is digitised by an analogue–to–digital converter (ADC) to form a sequence of phase samples. In a parallel path, the magnitude component is digitised by a second, synchronised ADC, digitally processed to obtain a sequence of coefficients characterising the normalised envelope variations and this is then combined with corresponding (in time) samples of the phase sequence to form a single, composite sequence characterising both the phase and amplitude variations of the received radio frequency signal. This composite sequence is then processed by a digital demodulator/equaliser to recover the transmitted data.

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